REMARKS

Claims 20 to 38 are pending. Claims 20, 21, 26, 28, 30, and 35 to 38 have been amended by this amendment.

Objections to claims 20, 21 and 36 were made and specific corrections were required by the Examiner. The corrections have been made and, therefore, withdrawal of the objections to claims 20, 21 and 36 is respectfully requested.

Minor amendments to claims 26, 28, 30, 37, and 38 have been made to add omitted punctuation. In addition, claims 20 and 35 have been amended to better emphasize the environment and hence the novelty of the claimed invention. Specifically, claim 20 has been amended to recite a "bus power-supply device *in a node for connection to a serial bus*, said bus power-supply device structured to supply power from a power-supply voltage of a node of a proceeding stage to a node of a next stage through the serial bus connected to said node by a physical layer and a plurality of connectors conductive to each other of the node" and "communication being *maintained* between said node and proceeding and next stages through the serial bus *whether a power-supply voltage is supplied or not*" (emphasis added).

Claims 20 to 38 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,351,818 to Murai. This rejection is respectfully traversed for the reason that Murai neither shows nor suggests the claimed invention.

The claimed invention is directed to supplying power supply voltage mutually in relation to three or more nodes connected through a serial bus. The preferred embodiments of the invention are improvements of the IEEE-1394 Standard. In the embodiment shown in Figure 1, the bus power-supply device 10 of the node 100 includes a power-supply circuit 2, a voltage detection unit 3, a selector 4, and a DC-DC converter 5. The power-supply circuit 2 and power-supply terminals 81 and 91 of respective connectors 8 and 9 are connected through a diode 7 for preventing reverse current from the terminals 81 and 91 to the power-supply circuit 2. The voltage detection unit 3 detects supply/non-supply of

a power-supply voltage from input terminal 1. The selector 4 is controlled by the voltage detection unit 3 to switch either a DC voltage output from the power-supply circuit 2 or a DC voltage from the terminals 81 and 91 to the physical layer 6 through the DC-DC converter 5. Thus, when no power-supply voltage is supplied to the power-supply circuit 2, the selector 4 supplies a DC voltage applied from the bus power source through the serial bus via terminals 81 and 91 to the physical layer 6. On the other hand, when a power-supply voltage from the internal power source is supplied to the power-supply circuit 2, the selector 4 cuts off the path from supplying a DC voltage from the serial bus to the physical layer and supplies the output of the power-supply circuit 2 to the physical layer 6.

The second embodiment, shown in Figure 2, is similar but adds a diode 13 between the power-supply circuit 2 and the DC-DC converter 5 and substitutes a transistor 41 for the selector. The first electrode 41a of the transistor 41 is connected to the terminals 81 and 91. The second electrode 41b of the transistor 41 is connected to the physical layer 6 through the DC-DC converter 5. The third electrode 41c of the transistor 41 is connected to the output of the voltage detection means 3. The two paths for supplying current to the DC-DC converter 5 are labeled A and B. When power is supplied from the power-supply voltage input terminal 1, the second path B is cut off by transistor 41 under control of the voltage detection means 3. On the other hand, when no power-supply voltage is supplied to terminal 1, transistor 41 conducts to supply DC voltage from terminals 81 and 91 to DC-DC converter 5. In this case, the diode 13 blocks reverse current to the power-supply circuit 2.

The third embodiment, shown in Figure 3, is similar to the embodiment of Figure 2, but substitutes a comparator 31 for the voltage detection means 3. The comparator 31 compares a reference voltage applied to terminal 30 to an output voltage of the power-supply circuit 2 and provides an output to control the conduction or non-conduction of transistor 41.

The fourth embodiment, shown in Figure 4, is similar to the first embodiment of Figure 1, but substitutes a relay 15 for the voltage detection means 3 and selector 4. When a power supply voltage is applied from the power-supply

circuit 2 to the main body 15b of the relay 15, the relay contract 15a is displaced from the position shown in Figure 4 to connect the output of the power-supply circuit 2 to the DC-DC converter 5. On the other hand, when no power supply voltage is applied from the power-supply circuit 2 to the main body 15b of the relay 15, the relay contact 15a reverts to the position shown in Figure 2, connecting terminals 81 and 91 to the DC-DC converter 5.

As shown in Figures 1 and 2, Murai discloses an external IEEE-1394 interface circuit in computer system 1 which is capable of continuing data communication between other electronic devices 7 and 8 having IEEE-1394 interfaces through the computer system 1 even when a main body power source 2 in the computer system 1 is cut off. The interface of the computer system 1 has a power source control portion 4, a link layer control portion 5 and a physical layer control portion 6. In the power source control portion 4, a power source detecting portion 41 and a switch 42 are arranged. When an input of power from the main body power source 2 is detected, as generally indicated in Figure 1, the power source detecting portion 41 of the power source control portion 4 controls the switch 42 so that the power from the main body power source 2 is supplied to the physical layer control portion 6. When input of power from the main body power source 2 is not detected, as generally indicated in Figure 2, the power source detecting portion 41 controls the switch 42 for supplying power from a power source of two external devices 7 and 8 having IEEE-1394 interfaces to the physical layer control portion 6 of the computer system.

As shown in Figure 1, while the main body power source 2 is turned ON, the link layer control portion 5 is driven by the main body power source 2. On the other hand, since the power source detecting portion 41 of the power source control portion 4 detects inputting of the main body power source 2, the switch 42 is controlled so that the main body power source 2 is supplied to the physical layer control portion 6. Therefore, in the interface 3, data communication can be performed between the external devices 7 and 8 through the IEEE-1394 physical layer control portion 6 and signal lines 111 and 112. On the other hand, it is also possible to perform data communication between the external devices 7 and 8

through a signal line 113 in certain specification of the interface 3.

On the other hand, as shown in Figure 2, when the main body power source 2 is turned OFF, the link layer control portion 5 is not driven. However, if inputting of the main body power source is not detected by the power source detecting portion 41, the switch 42 is controlled so that the power source of any one of the external devices 7 and 8 connected to the interface 3 is supplied to the physical layer control portion 6. Therefore, in the interface 3, data communication between the external devices 7 and 8 is cut off. However, data communication between the external devices 7 and 8 by the signal line 113 can be continued without being cutting off.

Notice that in the condition of the main body power source 2 being turned OFF, the computer system 1 is no longer in the communication chain. The computer system interface according to Murai is intended to insure only that the communication between devices 7 and 8 can continue through signal line 113. There is no longer communication between the devices 7 and 8 and the physical layer control portion 6, as clearly indicated by the X's on signal lines 111 and 112.

As can be seen, the present invention and the interface circuit of Murai, while sharing compatibilities with the IEEE-1394 standard, address two different problems. On the one hand, the present invention is concerned with devices connected in a serial bus line, as generally shown in Figure 5. A problem arises when the devices at the several nodes have power supplies of differing voltages, which can occur under the IEEE-1394 standard. The present invention enables relaying of a DC voltage applied from a serial bus when a node has an internal power source and prevents application of a DC voltage from another node to the physical layer of the device. On the other hand, when a node does not have an internal power source or the node's internal power source fails, a DC voltage from the serial bus is applied to the physical layer of the node.

In contrast, Murai does not contemplate such a serial bus line, but merely shows a computer system having attached two devices. No consideration is given to the possibility of the attached devices having power supplies of differing voltages under the IEEE-1394 standard. In fact, there is no discussion of the

presence (or absence) of internal power supplies of the two devices.

In the description of Murai, the physical connection and the connection on operation (path of a signal) are mixed up. In the description of Murai, not the physical connection, but the connection on operation is mainly explained.

In Figures 1 and 2 of Muari, since the power supply is not supplied to a link layer, a data communication between the interface 3 and the device 7, and the interface 3 and the device 8 is shut off. Therefore, the X marks are indicated on the signal lines 111 and 112 of Figure 2.

If it is assumed that the power supply is supplied to the physical layer, the signal lines 111 and 112 will be connected via the physical layer. In that case, the communication link between the devices 7 and 8 is possible via the signal line 113. However, it is explained below that the signal line 113 does not exist physically in Murai.

Although Murai explains the daisy chain connection between the device 7, interface 3, and device 8, its description of the daisy chain connection in Figures 1 and 2 is inaccurate. The correct physical daisy chan connection in Figure 1 of Murai is as follows.

As the daisy chain connection indicated in Figure 1 of Murai between the device 7 and the interface 3 and the device 8 is connected by one power supply line and signal line (111, 112). The signal line 113 which is described in Figures 1 and 2 of Murai does not exist. Therefore, when the signal lines 111 and 112 are cut off, the communication link between the devices 7 and 8 will be shut off.

About the voltage of the electronic power supply supplied to a serial bus, since the range of the voltage of the bus power supply specified in the IEEE-1394 standard is wide, a problem may arise in operation by the bus power supply. When supplying the serial bus power supply to the physical layer, after voltage is stabilized by the regulator, supplying the physical layer is described in the IEEE-1394 standard.

The claimed invention is provided with the DC-DC converter (the regulator) for stability of supply voltage. However, in Murai, there is no description about the voltage and the above-mentioned DC-DC converter of the

bus power supply.

The following description is found in Murai (col. 4, lines 23–29):

> "It should be noted that while the foregoing discussion has been given for the embodiment, in which the power source control portion 4, the link layer control portion 5 and the physical layer control portion 6 are arranged only in the interface 3, it is possible to construct the IEEE-1394 interfaces arranged in the external devices 7 and 8 with the same construction as the interface 3."

When the interface 3 is constructed so that it does not supply the internal power source to the serial bus as the IEEE-1394 interface of devices 7 and 8, power supply is supplied to the serial bus from neither a computer 1 nor the devices 7 or 8. Therefore, the above-mentioned description of Murai shows that the consideration about the power supply is not made.

About the problem stated in col. 1, lines 47–66, of Murai, the IEEE-1394-1995 standard has the following descriptions about the bus power supply:

The structure of this bus power supply of IEEE-1394-1995 standard is the same structure as Figure 6 of this application.

In the figure, OR connection of the internal power source and the serial bus power supply is made as a PHY power supply, and even when the internal power source is not supplied, a power supply is supplied to the physical layer from the serial bus.

In col. 1, lines 47–66 of Murai, it is described that the power source of the control portion is turned off when the internal power source is not supplied, and the communication between the devices through the daisy chain connection is shut off. However, the problem which is pointed out in Murai does not exists in the IEEE-1394-1995 standard.

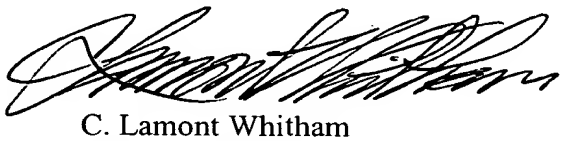
Each of independent claims 20 and 35 have been amended to recite "communication being maintained between said node and proceeding and next stages through the serial bus whether a power-supply voltage is supplied or not". This is not accomplished by Murai. As mentioned, the Murai interface circuit and the claimed invention are compatible with the IEEE-1394 standard and could be used together, but they are not interchangeable as they address different problems.

In view of the foregoing, it is respectfully requested that the application be reconsidered, that claims 20 to 38 be allowed, and that the application be passed to issue.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

A provisional petition is hereby made for any extension of time necessary for the continued pendency during the life of this application. Please charge any fees for such provisional petition and any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,



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